20. (Currently Amended) The method of generating of Claim 16 wherein said step of converting comprises the substeps of:

performing a digital to analog conversion on the analog waveform to generate a digital signal; and

generating the binary [[digital]] clock signal of the selected frequency from the digital signal using a phased-locked loop.

Remarks/Arguments

In response to the Office Action mailed June 1, 2005, Applicant respectfully requests that the Examiner reconsider the objections to the specification and the claims.

Claims 1 - 20 remain.

Claims 1 - 8, 9 – 16, and 20 are being amended.

Applicant has amended the specification and claims, as set forth above, to correct various informalities identified by the Examiner.

Claims 1, 3, 4-9, 14, and 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Corry et al.* (U.S. Patent 5,563,535) (hereinafter "the *Corry* reference"), in further view of *Dairi* (U.S. Patent 6,515,526) (hereinafter "the *Dairi* reference"). Applicant respectfully traverses these rejections.

Applicant respectfully submits that the *Corry* and the *Dairi* references, either taken alone or in combination, do not disclose or suggest clock generation circuits and methods which generate a digital signal by indexing a memory, converting that digital signal into an analog signal, filtering the analog clock signal to reduce clock jitter in a

binary output clock being derived therefrom, and then converting the filtered analog signal to generate the binary output signal signal having a rate near an integer multiple of a rate of the analog clock signal. Consequently, neither the *Corry* reference nor the *Dairi* reference, taken alone or in combination, achieves the substantial advantages realized by the embodiments of the present inventive principles.

One particular advantage provided by application of the present inventive principles is the minimization of both the output clock signal jitter and reference clock signal feed-through typically found in conventional phase locked loop (PLL) based signal generation circuits. In particular, as set forth in paragraph [0004] of the present application, the design of a typical PLL-based clock generation circuit requires a trade-off between minimizing jitter and minimizing reference clock feed-through. In other words, in a typical PLL-based signal generation system, reducing clock jitter generally requires accepting increased reference clock feed-through, and vice versa.

The *Corry* reference does not disclose or suggest generating a reduced-jitter binary output clock signal substantially at the rate of an analog clock signal from which the binary output clock signal is derived. Specifically, the *Corry* reference only discloses a system that generates an analog clock signal from a digital clock signal. Consequently, this reference does not consider the problem of reducing jitter during binary clock signal generation while at the same time minimizing reference clock feed-through. Instead, the *Corry* reference is addressing the problem of minimizing the size of the look up table (LUT) in a direct digital synthesis (DDS) circuit, while at the same maximizing accuracy of the waveform samples output from the LUT and input into a following digital to analog converter (DAC).

The *Dairi* reference also does not disclose or suggest generating a reduced-jitter binary output clock signal having a rate which is a multiple of the rate of an analog clock signal from which the binary output clock signal is derived. Specifically, the system disclosed in the *Dairi* reference generates a multiple-bit digital output signal with analog

to digital converter 64 shown in Figure 3. Furthermore, the rate of this multiple-bit digital output signal is substantially the sampling rate of analog to digital converter 64, rather than the rate of the sine waveform output from preceding direct digital synthesizer 61.

Claims 3 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the *Corry* and *Dairi* references, in further view of *Sheffer et al.* (U.S. Patent 4,951,004) (hereinafter "the *Sheffer* reference"). Applicant also respectfully traverses these rejections.

As with the *Corry* and *Dairi* references, the *Sheffer* reference does not teach or suggest generating a reduced-jitter binary output clock signal having a rate near an integer multiple of a rate of an analog clock signal from which the binary output clock signal is derived. Instead, the *Sheffer* reference only discloses a system in which a PLL 20, including a feedback path binary phase accumulator 23, provides an analog input signal into a direct digital synthesizer (DDS) 30, as shown in Figure 3. DDS 30 generates an analog output waveform.

In sum, since the *Corry*, *Dairi*, and *Sheffer* references, taken either alone or in combination, do not teach or suggest generating a reduced-jitter binary output clock signal having a rate which is near an integer multiple of an analog clock signal from which the binary output clock signal is generated, Applicant respectfully requests that the rejections of the claims be withdrawn.

No new matter has been added; the claims have been merely amended to more particularly claim the subject matter Applicant believes is inventive. Applicant respectfully submits that the Claims as they now stand are patentably distinct over the art cited during the prosecution thereof.

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Applicant respectfully requests a First Month Extension of Time to File this Response. Enclosed with this paper is Form PTO/SB/22 with Extension Fees in the amount of $120.

With the addition of no new claims, no additional filing fees are due. However, the Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account Number 20-0821 of Thompson & Knight LLP.

If the Examiner has any questions or comments concerning this paper or the present application in general, the Examiner is invited to call the undersigned at (214) 969 - 1749.

Respectfully submitted,

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